



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/789,479	02/26/2004	Kie Y. Ahn	500466.03 (29356/US/2)	8444

7590 06/27/2005

Steven H. Arterberry, Esq.  
DORSEY & WHITNEY LLP  
Suite 3400  
1420 Fifth Avenue  
Seattle, WA 98101

EXAMINER

GUHARAY, KARABI

ART UNIT

PAPER NUMBER

2879

DATE MAILED: 06/27/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

fm

<b>Office Action Summary</b>	<b>Application No.</b> 10/789,479	<b>Applicant(s)</b> AHN ET AL.	
	<b>Examiner</b> Karabi Guharay	<b>Art Unit</b> 2879	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 15 April 2005.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 62-95 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 62-95 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 26 June 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \*    c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

Amendment, filed on 4/15/2005 has been considered and entered.

New claims 91-95 have been added.

In the preliminary Amendment of specification, please update the continuation information by including the patent number.

### ***Specification***

Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

Amendment of the Abstract is required.

### ***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 62-65, 68-75, 78-82 are rejected under 35 U.S.C. 103(a) as being unpatentable over Doan et al. (US 5186670) and in view of Lee (US 5458518).

Regarding claims 62-64, 68-70, 71-73 & 78-80, Doan discloses a field emission device (Fig 1) comprising a substrate (11 of Fig 1), a plurality of spaced apart conductors (12) formed on the substrate (11), a plurality of spaced apart emitter bodies (13) comprising a high resistivity material (lines 41-44 of column 4) formed on the conductors (lines 18-27 of column 3), a dielectric layer (14 of FIG 1) having respective openings coaxial with the emitter bodies (lines 38-41 of column 3), an extraction grid (15) formed on the dielectric layer including respective opening coaxial with the emitter bodies (see Fig 1, lines 27-29 of column 3), an emitter tip (13) formed on each of the emitter bodies in the extraction grid opening, the tip formed from a material (Ba or Ce) having work function less than 4 electron volt (lines 27-32 of column 6), and a cathodoluminescent coated (phosphor) faceplate (16 of Fig 1) having a planar surface formed parallel to and near the plane of tips of the plurality of emitters (see Fig 1) .

Doan further discloses that the dielectric layer (14 of Fig 1 or 18 of Fig 7) is made of silicon dioxide (line 50 of column 4), but fail to disclose porous silicon dioxide.

However, in the same field of field emitters, Lee discloses a field emission device where the dielectric layer is a porous silicon dioxide layer (24 of Fig 6) on a substrate (10, lines 52-64 of column 3) in order to improve the symmetry and the uniformity of the configuration surrounding the cathode tips (lines 16-19 of column 2). Moreover it is well known in the art that the porous silicon dioxide is a low dielectric constant material suitable as an interlayer dielectric for a micro electronic structure, thus Lee provides a lower turn on voltage for the filed emission device.

Thus, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate porous dielectric layer, as disclosed by Lee, in the device of Doan, since this will further reduce the consumption of power by the field emission device as well as provide uniformity of the configuration surrounding the cathode tips.

Furthermore Lee discloses a p-type semiconductor substrate, which undergoes through etching process but does not explicitly specify that the substrate is polycrystalline. However, it is well known in the art that polycrystalline character accelerate doping process and etching rate of polycrystalline substrate is also high. Thus it would have been obvious to one having ordinary skill in the art at the time the invention was made to choose polycrystalline substrate which will form a porous polycrystalline silicon layer, in the device of Lee, since it has been held to be within the general skill of a worker in the art to select polycrystalline silicon substrate for its intended use as it is more suitable for doping process and faster etching process.

Further, Lee discloses that the dielectric layer has porosity, but does not specifically disclose the percentage of porosity, however, it is well known that porous silicon oxide layer produced by anodization and then oxidation of a silicon layer has the property of having density of 20% to 80% of that bulk density in other words 20% to 80% void (see Yue et al. 5430300, lines 59-61 of column 1). Thus it would have been obvious to one having ordinary skill in the art at the time the invention was made to obtain a porous silicon oxide layer comprising 50% void, or voids between 22.5% to 61.5%, since it has been held that discovering an optimum value of a result, effective

Art Unit: 2879

variable involves routine skill in the art. Lee further does not explicitly disclose the relative dielectric constant of porous dielectric layer, however, it is known in the art that porous silicon oxide layer has a low dielectric constant and by controlling the porosity of the layer one can change the dielectric constant of the porous silicon oxide layer. Thus it would have been obvious to one having ordinary skill in the art at the time the invention was made to obtain a porous silicon oxide layer having relative dielectric constant less than 1.6, since it has been held that discovering an optimum value of a result, effective variable involves routine skill in the art.

Regarding claims 65, 75, Doan discloses that the emitter tip comprises a material chosen from a group consisting of: Sic, Zr, La, Zn, TiN, LaB<sub>6</sub>, Ce, Ba, diamond and silicon oxycarbide (lines 27-32 of column 6).

Regarding claims 74 and 81, Doan discloses an emitter body comprising a high resistivity material and emitter tip formed on the emitter and in the extraction grid opening (see rejection of claim 62).

Regarding claim 82, Doan discloses that the emitter tips comprises a material chosen from a group consisting of: Sic, Zr, La, Zn, TiN, LaB<sub>6</sub>, Ce, Ba, diamond and silicon oxycarbide (lines 27-32 of column 6), and emitter body comprises cermet material (line 30 of column 6).

Claims 66, and 76 are rejected under 35 U.S.C. 103(a) as being unpatentable over Doan and Lee as applied to claim 1 above, and further in view of Jones (US 5869169).

Regarding claims 66 & 76, Doan and Lee meet all the limitations of the claim 8 except for the limitation of the emitter body being comprised of silicon monoxide and a metal. However, Jones discloses a field emitter element comprising SiO and a metal (Cr see abstract). This particular type of emitter element minimizes the susceptibility of the gate to stress (lines 44-47 of column 1).

Thus, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate emitter element, as disclosed by Jones, in the combined structure of Doan and Lee, since this will reduce the stress and cracking of gate element.

Claims 67,77 & 83 are rejected under 35 U.S.C. 103(a) as being unpatentable over Doan and Lee and Jones as applied to claim 8 above, and further in view of Itoh et al. (US 5793154).

Regarding claims 67, 77 and 83, Doan, Lee and Jones together disclose all the limitations of claim 67,77, & 83 except for the limitation of emitter body being comprised of manganese. However, Itoh et al. disclose a field emission element (28 of Fig 3) comprising manganese (lines 7-8 of column 3) in order to minimize the production of any oxide layer on the tip surface of the emitter (lines 27-31 of column 2).

Thus, it would have been obvious to one having ordinary skill in the art at the time the invention was made to include manganese metal in the emitter body as disclosed by Itoh et al., in the modified structure of Doan and Lee and Jones, since this will minimize the production of oxide layer on the tip of the emitter, thus will provide a

field emission element capable of stable and satisfactory emission characteristics for a long period of time.

Though Itoh et al. specifically do not disclose the percentage of manganese present in the emitter body, optimization of prior art structure is considered to be within the general skill of a worker in the art.

Claims 84-88, & 90 are rejected under 35 U.S.C. 103(a) as being unpatentable over Thoeny et al. (US 5473222), in view Doan and Lee (US 5458518).

Regarding claim 84-86, Thoeny et al. discloses a computer system (see Fig 4) comprising a central processing unit, a memory device, an input interface and a display (active matrix anode array of Fig 4). But Thoeny et al. do not disclose a field emission display device having limitations as of claims 84-86.

However Combines structure of Doan and Lee discloses a field emission device having all the limitations of claims 84-86 (see rejection of claim 62-64). This particular field emission display provides a low consumption of power for having a porous silicon oxide layer of low dielectric constant.

Thus, it would have been obvious to one having ordinary skill in the art at the time the invention was made to replace a display device, as disclosed by Doan and Lee, in the device of Theony, since this will reduce the consumption of power.

Regarding claim 87, Both Doan and Lee disclose an emitter body comprises a high resistivity material (silicon oxide) including an emitter tip in the extraction grid (see Fig 2 of Doan et al. or Fig 6 of Lee). The same reason for combining art as claim 84 applies.



Claim 88 recites essentially the same limitations of claim 65. Thus claim 88 is rejected as claim 65 (see rejection of claim 65).

Regarding claim 90, Doan discloses that the emitters are formed of materials having work function of less than 4 (lines 27-32 of column 6).

Claim 89 is rejected under 35 U.S.C. 103(a) as being unpatentable over Thoeny et al. (US 5473222), Doan and Lee (US 5458518) and further in view of Jones and Ito as in claim 67.

Claim 89 recites essentially the same limitations of claim 83. Thus claim 89 is rejected as claim 83 (see rejection of claim 83).

Regarding claims 91-95, lee et al. disclose that the after forming the porous silicon dioxide layer the layer has been etched back to a particular thickness then gates are formed on the porous silicon layer, since porous silicon layer has a predetermined thickness throughout with respect to the tip, thickness of the porous silicon layer is uniform and having a planarized upper surface on which the gate is formed (lines 40-46 of column 4 & lines 2-7 of column 5).

### ***Double Patenting***

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Art Unit: 2879

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claim 62, 71-80, 84-86 are is rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 1, 4-5, 7-9, 45-46 of U.S. Patent No. 6710538.

Although the conflicting claims are not identical, they are not patentably distinct from each other because

Claim 62 is anticipated by claim 4 of # 6710538,

Claim 71 is anticipated by claim 1 of # 6710538,

Claim 72 is anticipated by claim 4 of # 6710538,

Claim 73 is anticipated by claim 5 of # 6710538,

Claim 74 is anticipated by claim 1 of # 6710538,

Claim 75 is anticipated by claim 7 of # 6710538,

Claim 76 is anticipated by claim 8 of # 6710538,

Claim 77 is anticipated by claim 9 of # 6710538,

Claims 78-79 & 84, 86 are anticipated by claim 45 of # 6710538,

Claims 80, 85 are anticipated by claim 46 of # 6710538.

### ***Response to Arguments***

Applicant's arguments filed 4/15/2005 have been fully considered but they are not persuasive.

First of all, applicant contends that Lee teaches away from forming a porous silicon dioxide layer by deposition technique, however, Lee teaches a way of forming porous silicon dioxide layer for serving a dielectric layer for the field emission device. Claims are directed to an apparatus or device having a porous silicon dioxide layer as the dielectric layer in a field emission. Doan uses a silicon dioxide layer as the dielectric layer, while Lee patent teaches the use of porous silicon dioxide layer as the dielectric layer for the field emission display, which has some advantages over the non-porous silicon dioxide layer. Method of forming, such as forming integrally with the substrate, or specific technique of forming are not the issue for non-obviousness from a prior art structure satisfying all the structural limitations of the claimed device. As a structure, porous silicon dioxide layer (24) of Lee patent is formed on the substrate (10) and separated from the substrate by the layer 24' (see Fig 2B, 2C, & Fig 6).

#### ***Contact Information***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Karabi Guharay whose telephone number is (571) 272-2452. The examiner can normally be reached on Monday-Friday 8:30 am - 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nimeshkumar D. Patel can be reached on (571) 272-2457. The fax phone number for the organization is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status

Art Unit: 2879

information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

*Karabi Guharay*  
Karabi Guharay  
Patent Examiner  
Art Unit 2879